CLAIMS

1. An integrated circuit, comprising:

at least one main circuit operable to perform one or more functions, and including at least one I/O node for receiving or transmitting an operating signal;

an active termination circuit having first and second MOSFETs of the same type coupled in series across a Vdd node of a first source potential and a Vss node of a second source potential, the at least one I/O node being coupled to a common node between the first and second MOSFETs; and

a control circuit operable to bias the first and second MOSFETs such that they exhibit a controlled impedance at the common node.

2. The integrated circuit of claim 1, wherein the first and second MOSFETs are of the N-channel type.

3. The integrated circuit of claim 2, wherein the first and second MOSFETs are of the P-channel type.

4. The integrated circuit of claim 1, wherein:

the control circuit includes a first gate control circuit operable to provide a first gate drive signal to a gate of the first MOSFET, and a second gate control circuit operable to provide a second gate drive signal to a gate of the second MOSFET; and

the first and second gate drive signals are such that a quiescent voltage potential of the common node is between the Vdd and Vss potentials.

5. The integrated circuit of claim 4, wherein the quiescent voltage potential of the common node is at about a midpoint between the Vdd and Vss potentials.

6. The integrated circuit of claim 5, wherein the quiescent voltage potential of the common node is substantially non-zero.

7. The integrated circuit of claim 4, wherein:

the first gate control circuit includes a first impedance coupled between the gate and a drain of the first MOSFET and a first current source coupled from the gate of the first MOSFET to the Vss node;

the second control circuit includes a second impedance coupled between the gate and a drain of the second MOSFET and a second current source coupled from the gate of the second MOSFET to the Vss node;

the control circuit includes a third current source coupled between the Vdd node and the common node; and

respective magnitudes of the first, second, and third current sources are controlled to achieve the controlled impedance and the quiescent voltage potential at the common node.

8. The integrated circuit of claim 7, wherein the first, second, and third current sources are voltage controllable and produce respective currents in response to a current command signal to achieve the controlled impedance and the quiescent voltage potential at the common node.

9. The integrated circuit of claim 8, wherein the control circuit further includes a scaled MOSFET coupled in series with a fourth current source from the Vdd node to the Vss node, a third impedance coupled from a drain to a gate of the scaled MOSFET, a fifth voltage controlled current source receiving the current command signal and being

coupled from the gate of the scaled MOSFET to the Vss node, and an operational amplifier operable to produce the current command signal based on a reference voltage and a voltage at a source of the scaled MOSFET.

10. The integrated circuit of claim 9, wherein a ratio of the magnitude of the reference voltage and the magnitude of the fourth current source is substantially the controlled impedance at the common node.

11. The integrated circuit of claim 9, wherein the scaled MOSFET is a scaled version of the first MOSFET.

12. The integrated circuit of claim 9, wherein:

the control circuit includes a voltage source operable to produce about 1/2 of the voltage potential between the Vdd and Vss nodes, and a reference resistor coupled from the voltage source to a sixth current source; and

the reference voltage is taken at a junction of the reference resistor and the sixth current source.

13. An active signal termination circuit, comprising:

a first N-channel MOSFET having a gate terminal, a drain terminal, a source terminal, and a bulk terminal, the source terminal and the bulk terminal being coupled to a common node, and the drain terminal being coupled to a Vdd node of a first source potential; and

a second N-channel MOSFET having a gate terminal, a drain terminal, a source terminal, and a bulk terminal, the source terminal and the bulk terminal being coupled to a Vss node of a second source potential, and the drain terminal being coupled to the common node; and

a control circuit operable to bias the first and second MOSFETs such that they exhibit a controlled impedance at the common node.

14. The circuit of claim 13, wherein the control circuit comprises:

a first gate control circuit including a first impedance coupled between the gate terminal and the drain terminal of the first N-channel MOSFET and a first current source coupled from the gate terminal of the first N-channel MOSFET to the Vss node;

a second control circuit including a second impedance coupled between the gate terminal and the drain terminal of the second N-channel MOSFET and a second current source coupled from the gate terminal of the second N-channel MOSFET to the Vss node; and

a third current source coupled between the Vdd node and the common node,

wherein respective magnitudes of the first, second, and third current sources are controlled to achieve the controlled impedance and the quiescent voltage potential at the common node.

15. The circuit of claim 14, wherein the first, second, and third current sources are voltage controllable and produce respective currents in response to a current command signal to achieve the controlled impedance and the quiescent voltage potential at the common node.

16. The circuit of claim 15, wherein the control circuit further includes a scaled MOSFET coupled in series with a fourth current source from the Vdd node to the Vss node, a third impedance coupled from a drain to a gate of

the scaled MOSFET, a fifth voltage controlled current source receiving the current command signal and being coupled from the gate of the scaled MOSFET to the Vss node, and an operational amplifier operable to produce the current command signal based on a reference voltage and a voltage at a source of the scaled MOSFET.

17. The circuit of claim 16, wherein a ratio of the magnitude of the reference voltage and the magnitude of the fourth current source is substantially the controlled impedance at the common node.

18. The circuit of claim 16, wherein the scaled MOSFET is a scaled version of the first N-channel MOSFET.

19. The circuit of claim 16, wherein:

the control circuit includes a voltage source operable to produce about 1/2 of the voltage potential between the Vdd and Vss nodes, and a reference resistor coupled from the voltage source to a sixth current source; and

the reference voltage is taken at a junction of the reference resistor and the sixth current source.

20. An active signal termination circuit, comprising:

a first P-channel MOSFET having a gate terminal, a drain terminal, a source terminal, and a bulk terminal, the drain terminal and the bulk terminal being coupled to a Vdd node of a first source potential, and the source terminal being coupled to a common node;

a second P-channel MOSFET having a gate terminal, a drain terminal, a source terminal, and a bulk terminal, the drain terminal and the bulk terminal being coupled to the

common node, and the source terminal being coupled to a Vss node of a second source potential; and

a control circuit operable to bias the first and second MOSFETs such that they exhibit a controlled impedance at the common node.

21. The circuit of claim 20, wherein the control circuit comprises:

a first gate control circuit including a first impedance coupled between the gate terminal and the drain terminal of the second P-channel MOSFET and a first current source coupled from the gate terminal of the second P-channel MOSFET to the Vdd node;

a second control circuit including a second impedance coupled between the gate terminal and the drain terminal of the first P-channel MOSFET and a second current source coupled from the gate terminal of the first P-channel MOSFET to the Vdd node; and

a third current source coupled between the Vss node and the common node,

wherein respective magnitudes of the first, second, and third current sources are controlled to achieve the controlled impedance and the quiescent voltage potential at the common node.

22. The circuit of claim 21, wherein the first, second, and third current sources are voltage controllable and produce respective currents in response to a current command signal to achieve the controlled impedance and the quiescent voltage potential at the common node.

23. The circuit of claim 22, wherein the control circuit further includes a scaled MOSFET coupled in series

with a fourth current source from the Vdd node to the Vss node, a third impedance coupled from a drain to a gate of the scaled MOSFET, a fifth voltage controlled current source receiving the current command signal and being coupled from the gate of the scaled MOSFET to the Vss node, and an operational amplifier operable to produce the current command signal based on a reference voltage and a voltage at a source of the scaled MOSFET.

24. The circuit of claim 23, wherein a ratio of the magnitude of the reference voltage and the magnitude of the fourth current source is substantially the controlled impedance at the common node.

25. The circuit of claim 23, wherein the scaled MOSFET is a scaled version of the first P-channel MOSFET.

26. The circuit of claim 23, wherein:

the control circuit includes a voltage source operable to produce about 1/2 of the voltage potential between the Vdd and Vss nodes, and a reference resistor coupled from the voltage source to a sixth current source; and

the reference voltage is taken at a junction of the reference resistor and the sixth current source.

27. A method, comprising biasing first and second series coupled MOSFETs of the same type such that they exhibit a controlled impedance at a common node thereof, wherein the first and second MOSFETs are coupled in series across a Vdd node of a first source potential and a Vss node of a second source potential, the common node being between the first and second MOSFETs.